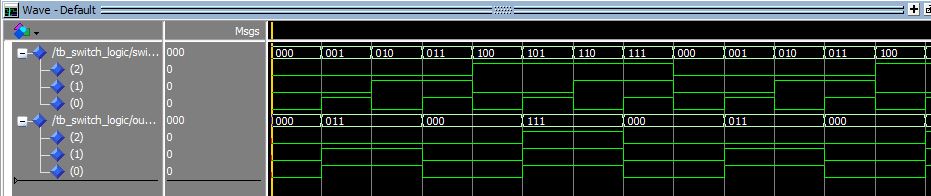
**Combinational Logic Timing Simulation:**



**Combinational and Sequential Logic Timing Simulation: (with a reset input as ‘0’ for 40ns and then as ‘1’ for 20ns):**

